CLAIMS

1. A method comprising:

dividing pins of an integrated circuit into a first group and a second group;

logically associating each pin of the first group to each pin of the second group; and

generating a scan chain in the integrated circuit for each logical association of pins.

2. The method of claim 1, further comprising:

driving the scan chains with the logical association of pins.

3. The method of claim 2, wherein the first group has n number of pins, the second group has m number of pins, and the logical association of pins drives n*m scan chains.

4. The method of claim 1, wherein logically associating comprises:

performing an exclusive OR operation.

5. The method of claim 4, wherein generating the scan chains comprises:

C[i][j] <= a[i] ExOR b[j]

where a[i] is a pin in the first group; b[j] is a pin in the second group; i = 1 to n; and j = 1 to m.

6. A method comprising:

dividing p pins of an integrated circuit into n groups;

logically associating the pins of each group through an ExOR matrix; and

driving a plurality of scan chains in the integrated circuit with the logically associated pins.

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7. The method of claim 6, wherein logically associating the pins further comprises:

generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

8. The method of claim 6, wherein the number of scan chains is equal to the number of logical associations.

9. The method of claim 6, wherein the ExOR matrix has n dimensions.

10. An apparatus comprising:

means for dividing pins of an integrated circuit into a first group and a second group;

means for logically associating each pin of the first group to each pin of the second group; and

means for generating a scan chain in the integrated circuit for each logical association of pins.

11. The apparatus of claim 10, further comprising:

means for driving the scan chains with the logical association of pins.

12. The apparatus of claim 11, wherein the first group has n number of pins, the second group has m number of pins, and the logical association of pins drives n*m scan chains.

13. The apparatus of claim 10, wherein said means for logically associating comprises:

means for performing an exclusive OR operation.

14. The apparatus of claim 13, wherein said means for generating the scan chains comprises:

means for determining **C[i][j] <= a[i] ExOR b[j]**

where a[i] is a pin in the first group; b[j] is a pin in the second group; i = 1 to n; and j = 1 to m.

15. An apparatus comprising:

means for dividing p pins of an integrated circuit into n groups;

means for logically associating the pins of each group through an ExOR matrix; and

means for driving a plurality of scan chains in the integrated circuit with the logically associated pins.

16. The apparatus of claim 15, wherein said means for logically associating the pins further comprises:

means for generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

17. The apparatus of claim 15, wherein the number of scan chains is equal to the number of logical associations.

18. The apparatus of claim 15, wherein the ExOR matrix has n dimensions.

19. An article of manufacture comprising:

a computer readable medium storing a computer program comprising:

code for dividing pins of an integrated circuit into a first group and a second group;

code for logically associating each pin of the first group to each pin of the second group;

code for generating a scan chain in the integrated circuit for each logical association of pins.

20. The medium of claim 19, wherein the program further comprises:

code for driving the scan chains with the logical association of pins.

21. The medium of claim 20, wherein the first group has n number of pins, the second group has m number of pins, and the logical association of pins drives n*m scan chains.

22. The medium of claim 19, wherein said code for logically associating comprises:

code for performing an exclusive OR operation.

23. The medium of claim 22, wherein said code for generating the scan chains comprises:

code for determining **C[i][j] <= a[i] ExOR b[j]**

where a[i] is a pin in the first group; b[j] is a pin in the second group; i = 1 to n; and j = 1 to m.

24. An article of manufacture comprising:

a computer readable medium storing a computer program comprising:

code for dividing p pins of an integrated circuit into n groups;

code for logically associating the pins of each group through an ExOR matrix; and

code for driving a plurality of scan chains in the integrated circuit with the logically associated pins.

25. The medium of claim 24, wherein said code for logically associating the pins further comprises:

code for generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

26. The medium of claim 24, wherein the number of scan chains is equal to the number of logical associations.

27. The medium of claim 24, wherein the ExOR matrix has n dimensions.